JIANGSU CHANGJIANG ELECTRONICS TECHNOLOGY CO., LTD

SOD-323 Plastic-Encapsulate Diodes

CESD12VD3 ESD Protection Diodes

SOD-323

DESCRIPTION

The CESD12VD3 is designed to protect voltage sensitive components from ESD. Excellent clamping capability, low leakage, and fast response time provide best in class protection on designs that are exposed to ESD. Because of its small size, it is suited for use in cellular phones, MP3 players, digital cameras and many other portable applications where board space is at a premium.

FEATURES

- Stand−off Voltage:3.3V−12 V
- Low Leakage
- Response Time is Typically < 1 ns
- ESD Rating of Class 3 (> 16 kV) per Human Body Model
- IEC61000−4−2 Level 4 ESD Protection
- These are Pb−Free Devices

Maximum Ratings @T_A=25℃

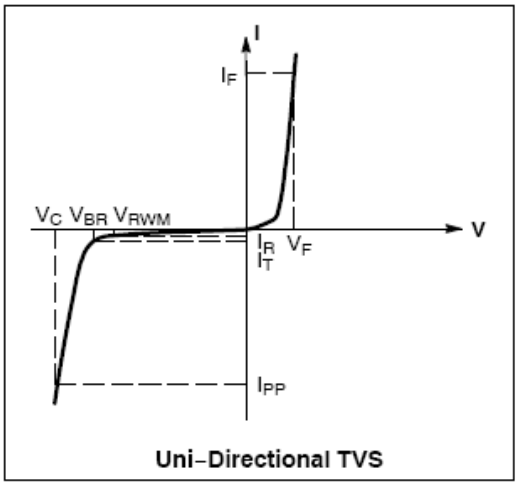
Parameter	Symbol	Limits	Unit
IEC61000−4−2(ESD) Air Contact		±15 ±8.0	KV
ESD voltage per human body model		30	KV
Total power dissipation on FR-5 board (Note 1)	P_D	200	mW
Thermal Resistance Junction−to−Ambient	$R_{\Theta JA}$	625	℃/W
Lead Solder Temperature − Maximum (10 Second Duration)	T_L	260	℃
Junction and Storage temperature range	T_j, T_{stg}	-55 ~ +150	℃

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended. Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR−5 = 1.0 x 0.75 x 0.62 in.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F
P_{pk}	Peak Power Dissipation
C	Max. Capacitance @V_R=0 and f =1MHz



Uni−Directional TVS

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted, V_F = 0.9 V Max. @ I_F = 10mA for all types)

Device*	Device Marking	V_{RWM} (V)	I_R (μ A) @ V_{RWM}	V_{BR} (V) @ I_T(Note 2)		I_T	Vc @IPP = 5 A	I_{PP}(A) +	V_C (V) @Max I_{PP}+	P_{pk} + (W)	C (pF)
		Max	Max	Min	Max	mA	V	Max	Max	Max	Typ
CESD3V3D3	YU	3.3	10	5.0	5.9	1.0	9.3	15	13.5	350	450
CESD5V0D3	ZA	5.0	10	6.2	7.3	1.0	9.8	15	15.5	350	350
CESD12VD3	ZC	12	1.0	13.3	15.75	1.0	22	12	33	350	150

*Other voltages available upon request.

+Surge current waveform per Figure 6.

2. V_{BR} is measured with a pulse test current I_T at an ambient temperature of 25°C.

TYPICAL CHARACTERISTICS

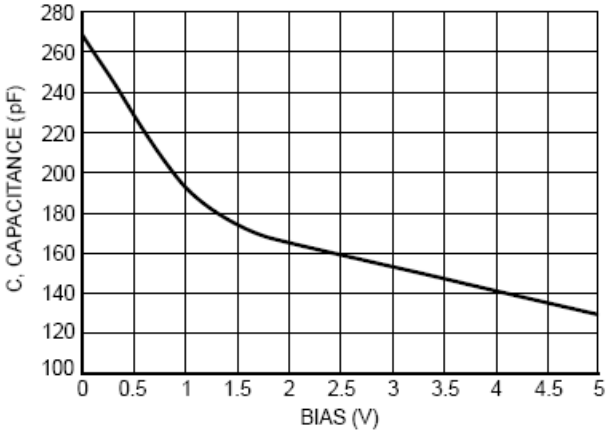


Figure 1. SD05 Typical Capacitance versus Bias Voltage

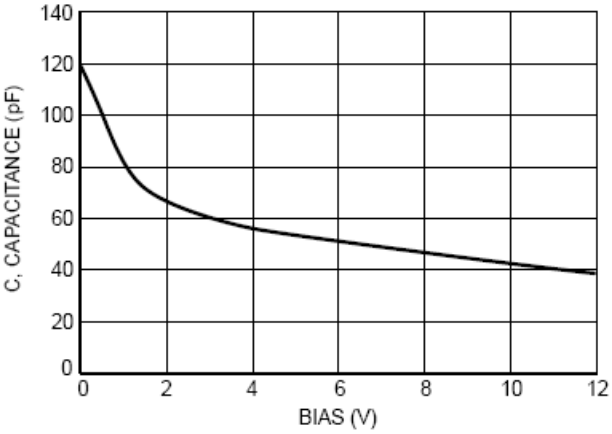


Figure 2. SD12 Typical Capacitance versus Bias Voltage

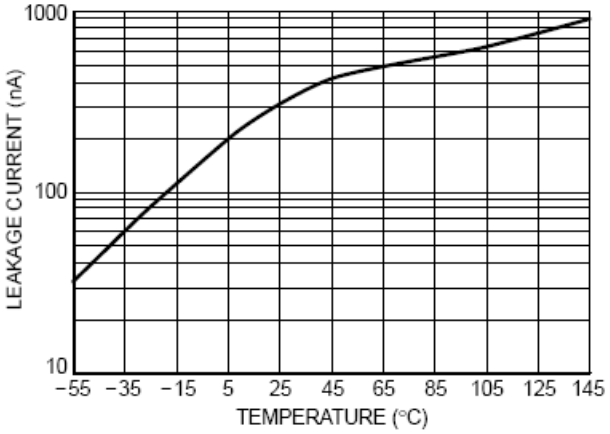


Figure 3. SD05 Typical Leakage Current versus Temperature

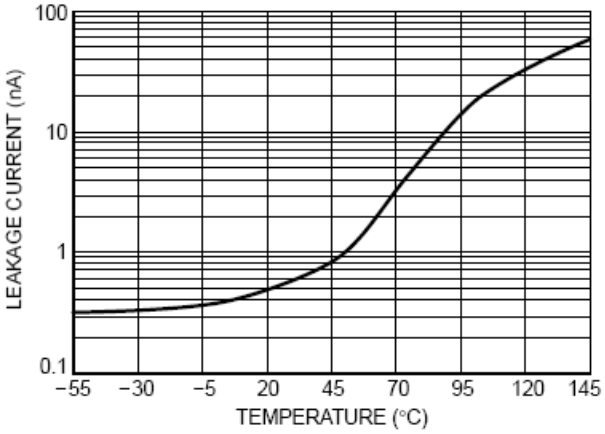


Figure 4. SD12 Typical Leakage Current versus Temperature

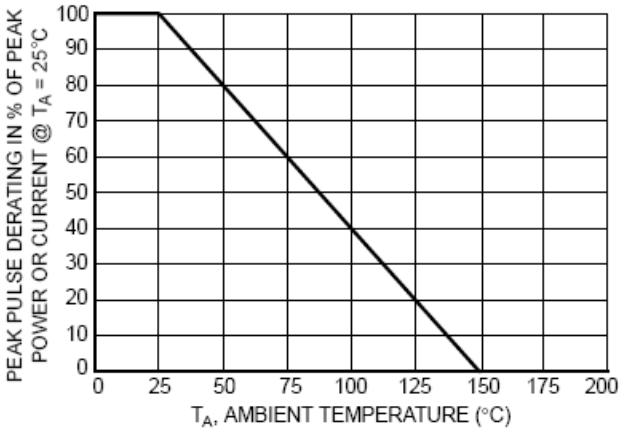


Figure 5. Pulse Derating Curve

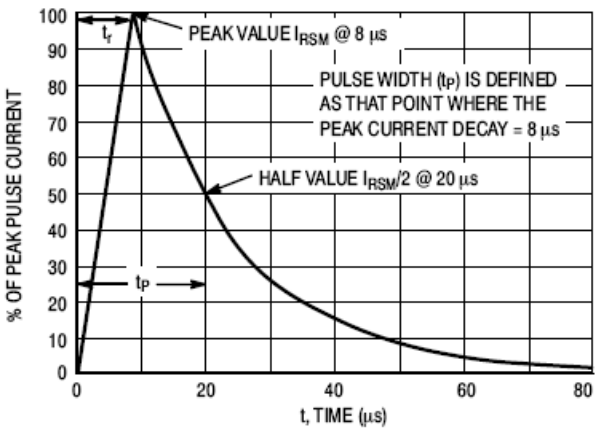


Figure 6. 8 × 20 μs Pulse Waveform