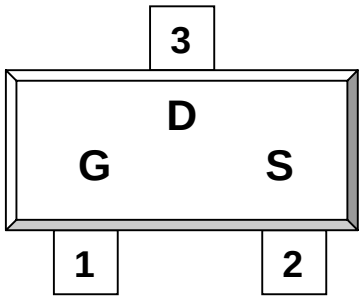
P Channel Enchancement Mode MOSFET 3409

-2.6A

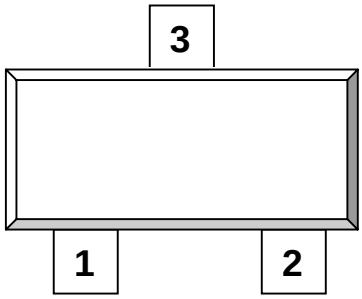
DESCRIPTION

The 3409 is the P-Channel logic enhancement mode power field effect transistor are produced using high cell density, DMOS trench technology.
This high density process is especially tailored to minimize on-state resistance.
These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other batter powered circuits, and low in-line power loss are needed in a very small outine surface mount package.

PIN CONFIGURATION
SOT-23-3L



1.Gate 2.Source 3.Drain



P Channel Enchancement Mode MOSFET 3409

-2.6A

ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-30	V
Gate-Source Voltage		V_{GSS}	+/-20	V
Continuous Drain Current (TJ=150℃)	T_A=25℃ T_A=70℃	I_D	-2.6 -2.2	A
Pulsed Drain Current		I_{DM}	-20	A
Continuous Source Current (Diode Conduction)		I_S	-1.25	A
Power Dissipation	T_A=25℃ T_A=70℃	P_D	1.4 1.0	W
Operation Junction Temperature		T_J	150	℃
Storgae Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	100	℃/W

P Channel Enchancement Mode MOSFET 3409

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250μA, V_{GS}=0V	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-30V, V_{GS}=0V			-1	μA
		T_J=55°C			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=-250μA	-1	-1.9	-3	V
$I_{D(ON)}$	On state drain current	V_{GS}=-4.5V, V_{DS}=-5V	-5			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V, I_D=-2.6A		97	130	mΩ
		V_{GS}=-4.5V, I_D=-2A		166	200	mΩ
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-2.5A	3	3.8		S
V_{SD}	Diode Forward Voltage	I_S=-1A,V_{GS}=0V		-0.82	-1	V
I_S	Maximum Body-Diode Continuous Current				-2	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-15V, f=1MHz		302	370	pF
C_{oss}	Output Capacitance			50.3		pF
C_{rss}	Reverse Transfer Capacitance			37.8	53	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	6	12	18	Ω
SWITCHING PARAMETERS						
Q_g(10)	Total Gate Charge(10V)	V_{GS}=-10V, V_{DS}=-15V, I_D=-2.6A		6.8	9	nC
Q_g(4.5)	Total Gate Charge(4.5V)			2.4	3.1	nC
Q_{gs}	Gate Source Charge			1.6		nC
Q_{gd}	Gate Drain Charge			0.95		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-10V, V_{DS}=-15V, R_L=5.8Ω, R_{GEN}=3Ω		7.5		ns
t_r	Turn-On Rise Time			3.2		ns
$t_{D(off)}$	Turn-Off DelayTime			17		ns
t_f	Turn-Off Fall Time			6.8		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-2.6A, dI/dt=100A/μs		16.8	22	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-2.6A, dI/dt=100A/μs		10		nC