



AO3404

N-Channel Enhancement Mode Field Effect Transistor

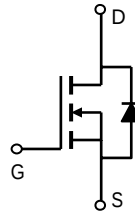
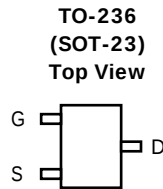
General Description

The AO3404 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device may be used as a load switch or in PWM applications. *Standard Product AO3404 is Pb-free (meets ROHS & Sony 259 specifications).*

Features

$V_{DS} (V) = 30V$
 $I_D = 5.8A (V_{GS} = 10V)$
 $R_{DS(ON)} < 28m\Omega (V_{GS} = 10V)$
 $R_{DS(ON)} < 43m\Omega (V_{GS} = 4.5V)$

R_g, C_{iss}, C_{oss}, C_{rss} Tested



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^A	I_D	5.8	A
$T_A=25^\circ C$		4.9	
Pulsed Drain Current ^B	I_{DM}	20	
Power Dissipation	P_D	1.4	W
		1	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	65	90	$^\circ C/W$
$t \leq 10s$		85	125	$^\circ C/W$
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	43	60	$^\circ C/W$
Steady-State				
Maximum Junction-to-Lead ^C	$R_{\theta JL}$			$^\circ C/W$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1	1.9	3	V
I _{D(ON)}	On state drain current	V _{GS} =4.5V, V _{DS} =5V	20			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =5.8A T _J =125°C		22.5 31.3	28 38	mΩ
		V _{GS} =4.5V, I _D =5.0A		34.5	43	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =5.8A	10	14.5		S
V _{SD}	Diode Forward Voltage	I _S =1A		0.76	1	V
I _S	Maximum Body-Diode Continuous Current				2.5	A
I _S	Pulsed Body-Diode Current ^B				20	A
DYNAMIC PARAMETERS						
C _{ISS}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		680	820	pF
C _{OSS}	Output Capacitance			102		pF
C _{RSS}	Reverse Transfer Capacitance			77	108	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	1.5	3	3.6	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =5.8A		13.88	17	nC
Q _g (4.5V)	Total Gate Charge			6.78	8.1	nC
Q _{gs}	Gate Source Charge			1.8		nC
Q _{gd}	Gate Drain Charge			3.12		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =2.7Ω, R _{GEN} =3Ω		4.6	6.5	ns
t _r	Turn-On Rise Time			3.8	5.7	ns
t _{D(off)}	Turn-Off DelayTime			20.9	30	ns
t _f	Turn-Off Fall Time			5	7.5	ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =5.8A, dI/dt=100A/μs		16.1	21	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =5.8A, dI/dt=100A/μs		7.4	10	nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any a given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using <30Qμs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

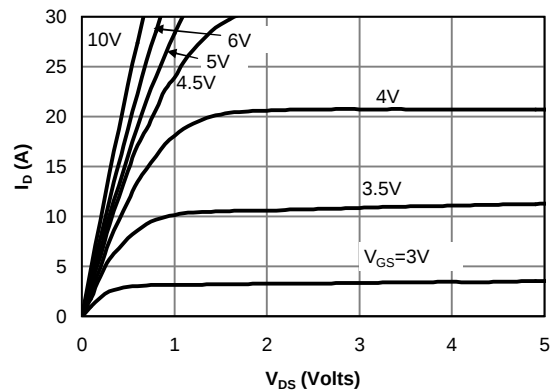


Fig 1: On-Region Characteristics

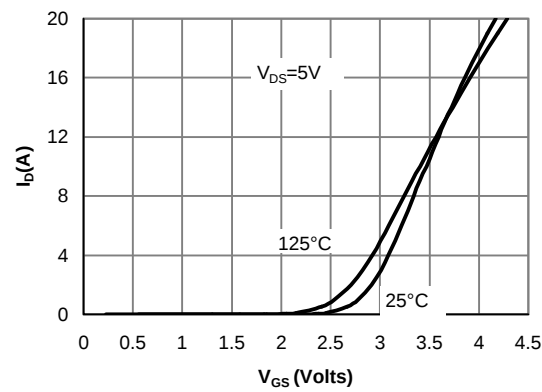


Figure 2: Transfer Characteristics

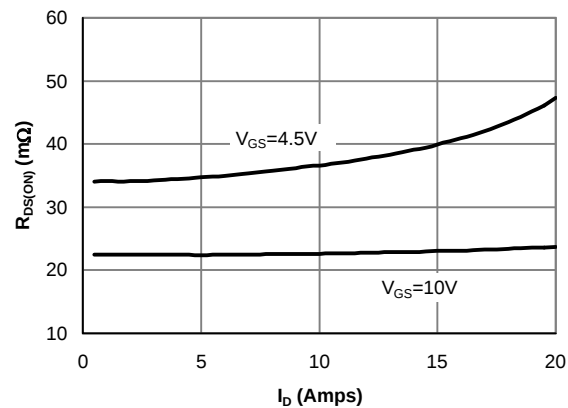


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

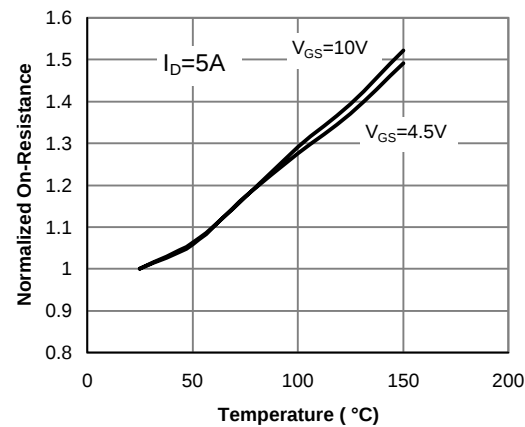


Figure 4: On-Resistance vs. Junction Temperature

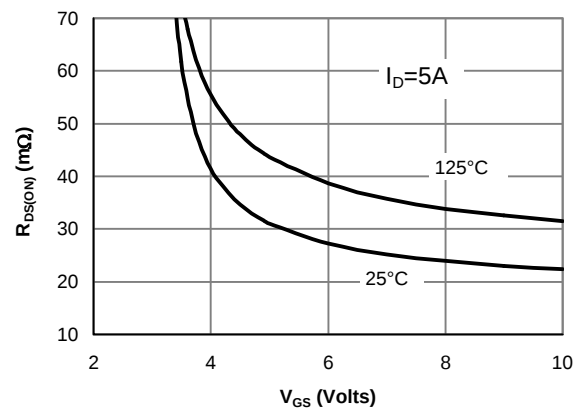


Figure 5: On-Resistance vs. Gate-Source Voltage

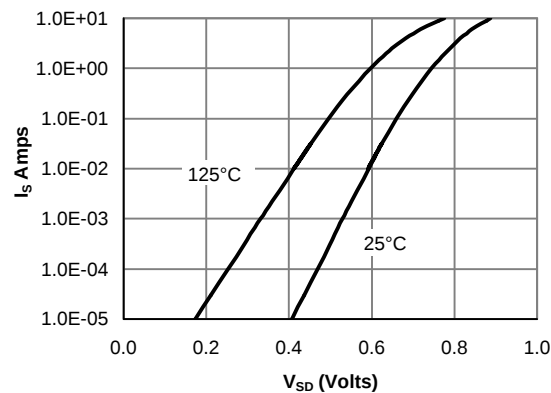


Figure 6: Body diode characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

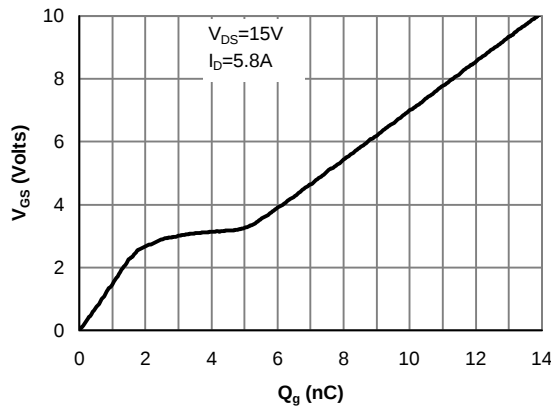


Figure 7: Gate-Charge characteristics

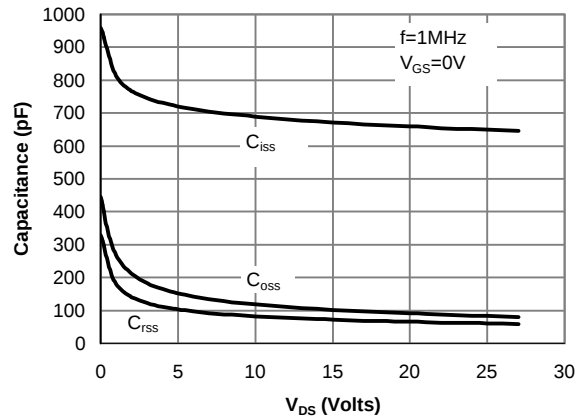


Figure 8: Capacitance Characteristics

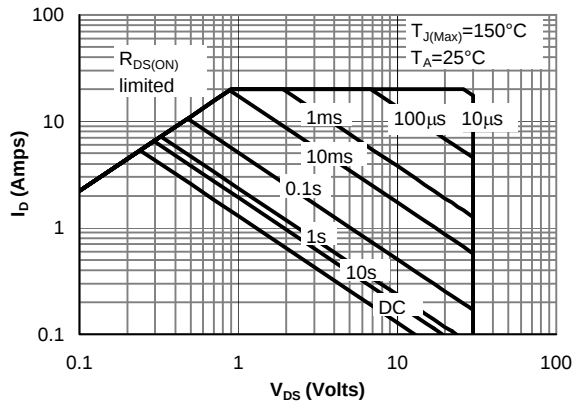


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

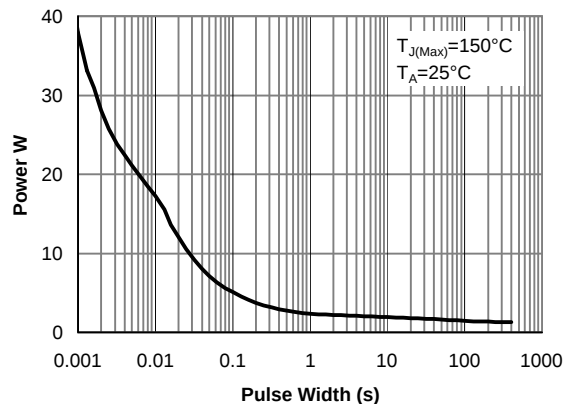


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

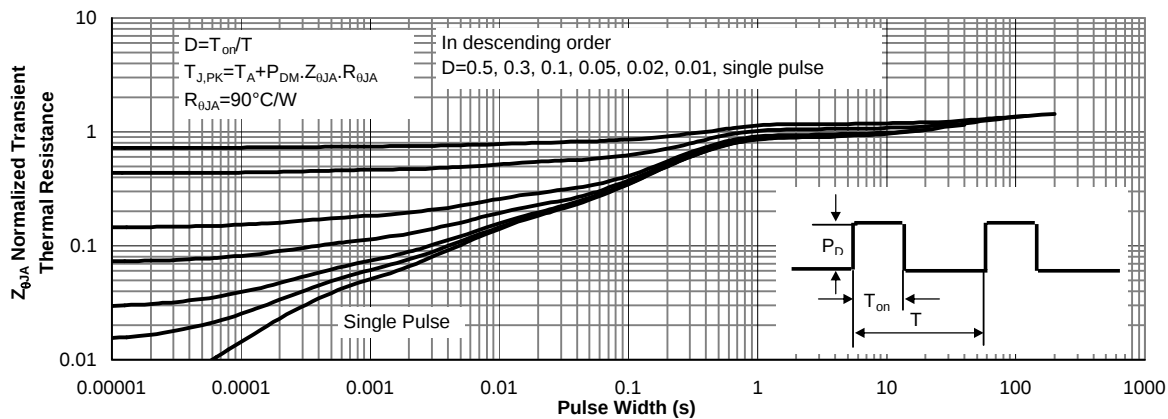


Figure 11: Normalized Maximum Transient Thermal Impedance