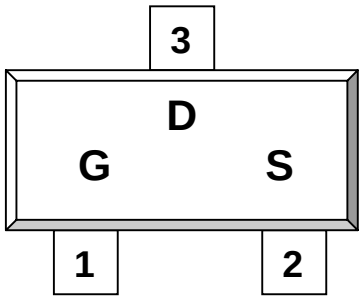
P Channel Enchancement Mode MOSFET 3403

-2.6A

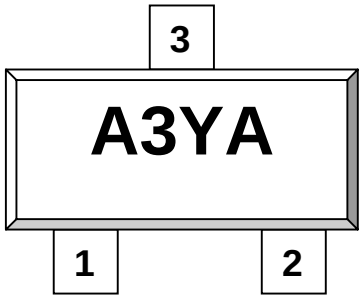
DESCRIPTION

The 3403 is the P-Channel logic enhancement mode power field effect transistor are produced using high cell density, DMOS trench technology.
This high density process is especially tailored to minimize on-state resistance.
These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other batter powered circuits, and low in-line power loss are needed in a very small outine surface mount package.

PIN CONFIGURATION
SOT-23-3L



1.Gate 2.Source 3.Drain



A3: Purduct Name Y: Year Code A: Process Code

P Channel Enchancement Mode MOSFET 3403

-2.6A

ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-30	V
Gate-Source Voltage		V_{GSS}	+/-20	V
Continuous Drain Current (TJ=150℃)	T_A=25℃ T_A=70℃	I_D	-2.6 -2.2	A
Pulsed Drain Current		I_{DM}	-20	A
Continuous Source Current (Diode Conduction)		I_S	-1.25	A
Power Dissipation	T_A=25℃ T_A=70℃	P_D	1.4 1.0	W
Operation Junction Temperature		T_J	150	℃
Storgae Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	100	℃/W

P Channel Enchancement Mode MOSFET 3403

-2.6A

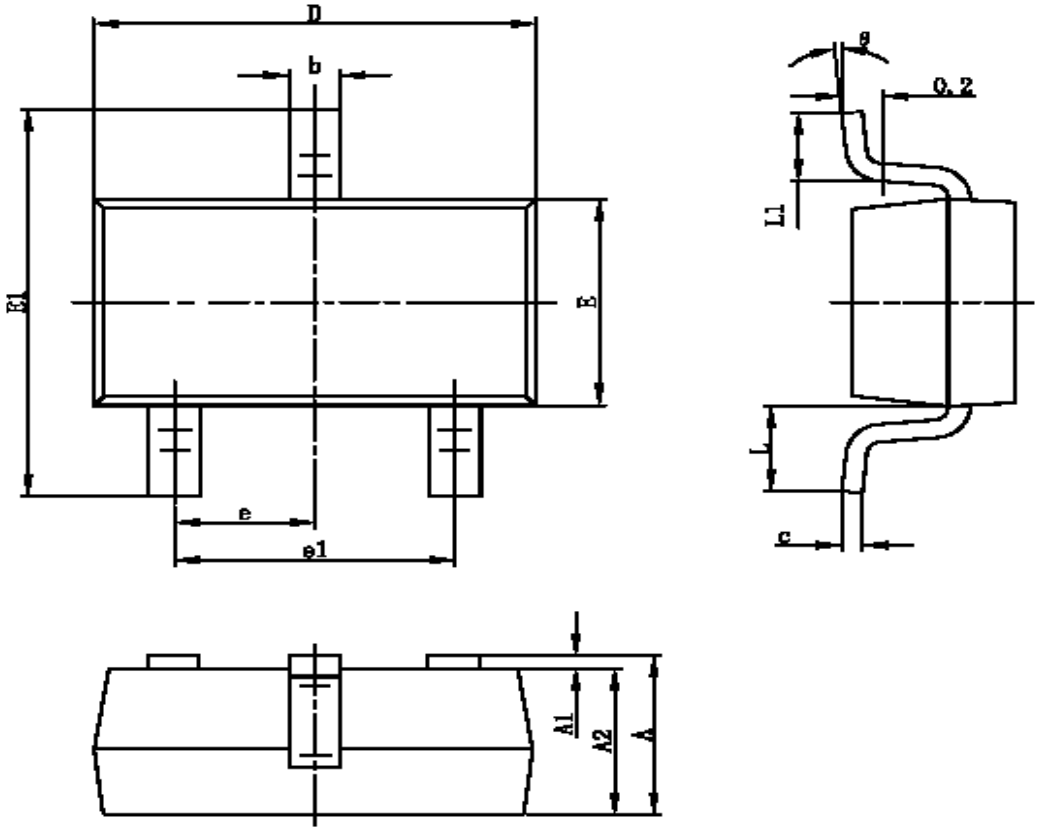
ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250uA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250uA	-0.6		-1.4	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=+20V			+100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V,V_{GS}=0V			-1	uA
		V_{DS}=-30V,V_{GS}=0V T_J=55℃			-5	
On-State Drain Current	$I_{D(on)}$	V_{DS}≦-5V,V_{GS}=-10V	-10			A
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-2.6A V_{GS}=-4.5V,I_D=-2.0A V_{GS}=-2.5V,I_D=-1.0A		0.103 0.128 0.187	0.130 0.180 0.260	Ω
Forward Transconductance	g_{fs}	V_{DS}=-5V,I_D=-2.5A	3.0	4.5		S
Diode Forward Voltage	V_{SD}	I_S=-1.0A,V_{GS}=0V		-0.85	-1.0	V
Dynamic						
Total Gate Charge	Qg	V_{DS}=-15V,V_{GS}=-4.5V I_D≡-2.5A		4.4	5.3	nC
Gate-Source Charge	Qgs			0.8		
Gate-Drain Charge	Qgd			1.32		
Input Capacitance	Ciss	V_{DS}=-15V,V_{GS}=0V F=1MHz		226		PF
Output Capacitance	Coss			87		
Reverse Transfer Capacitance	Crss			19		
Turn-On Time	$t_{d(on)}$	V_{DD}=-10V,R_L=6Ω V_{DS}=-15V, V_{GEN}=-3Ω		5.3	8	nS
	t_r			4.4	9	
Turn-Off Time	$t_{d(off)}$			31.5	45	
	t_f			8	16	

P Channel Enchancement Mode MOSFET 3403

-2.6A

SOT-23-3L PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

P Channel Enchancement Mode MOSFET 3403

-2.6A

TYPICAL CHARACTERICTICS (25℃ Unless noted)

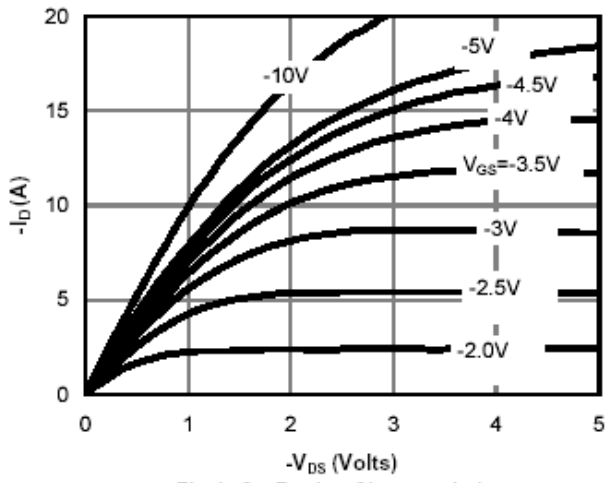


Fig 1: On-Region Characteristics

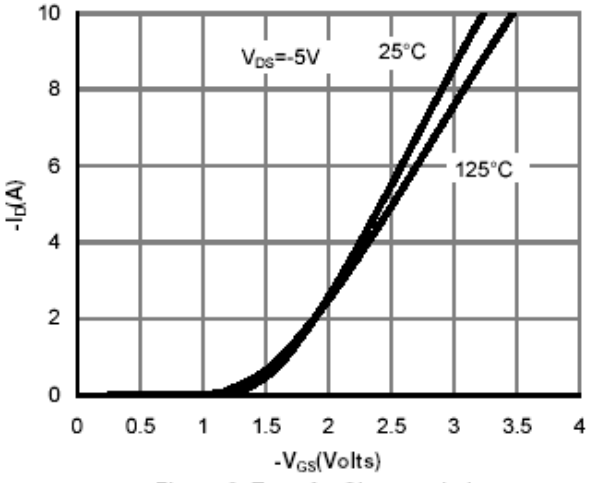


Figure 2: Transfer Characteristics

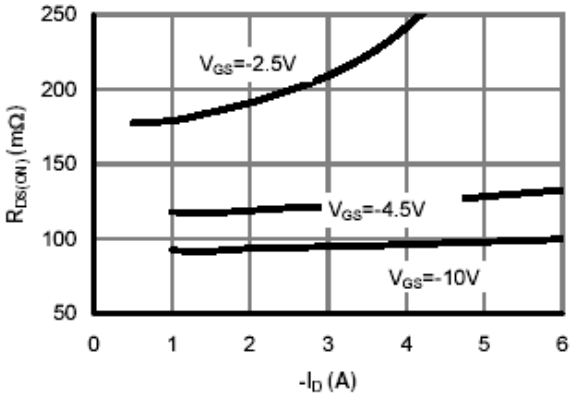


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

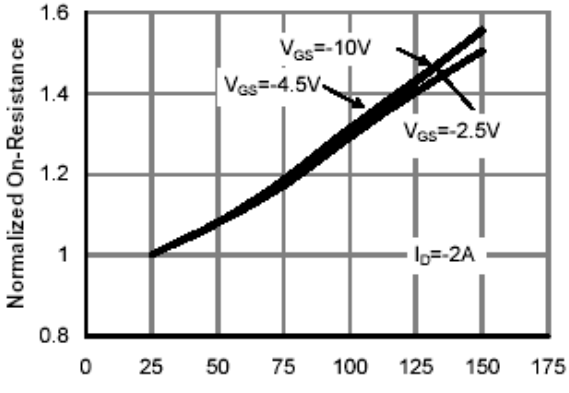


Figure 4: On-Resistance vs. Junction Temperature

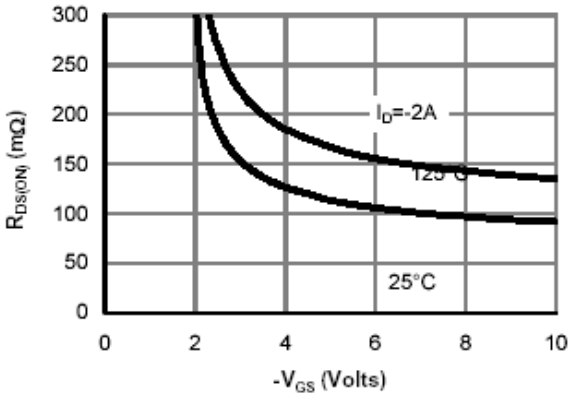


Figure 5: On-Resistance vs. Gate-Source Voltage

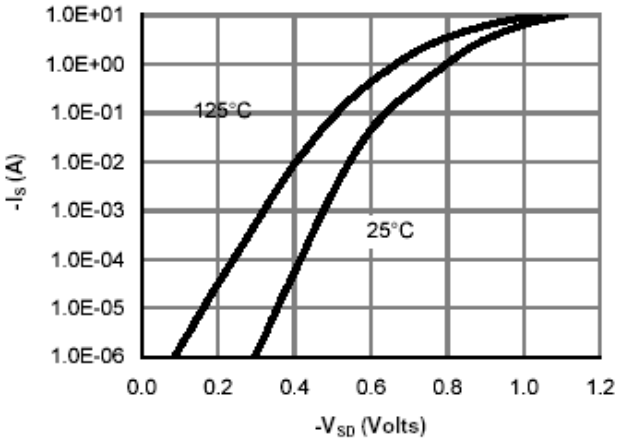


Figure 6: Body-Diode Characteristics

P Channel Enchancement Mode MOSFET 3403

-2.6A

TYPICAL CHARACTERICTICS (25℃ Unless noted)

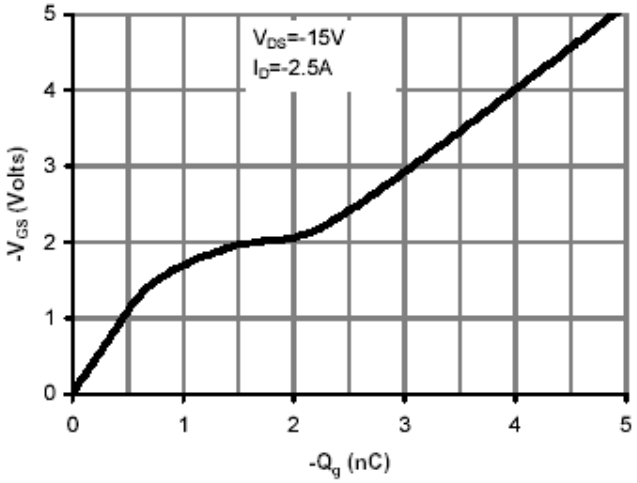


Figure 7: Gate-Charge Characteristics

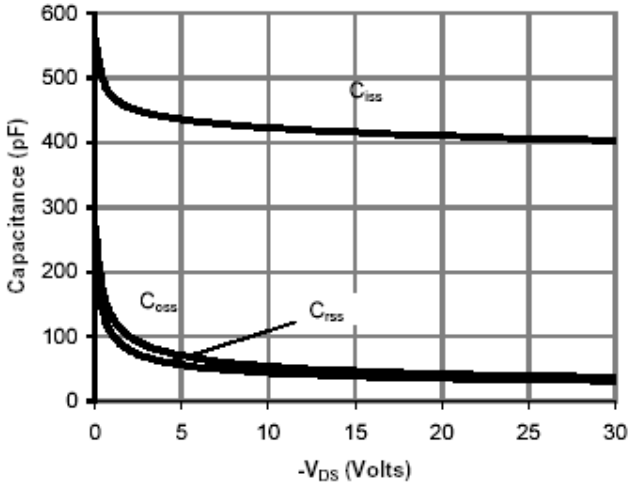


Figure 8: Capacitance Characteristics

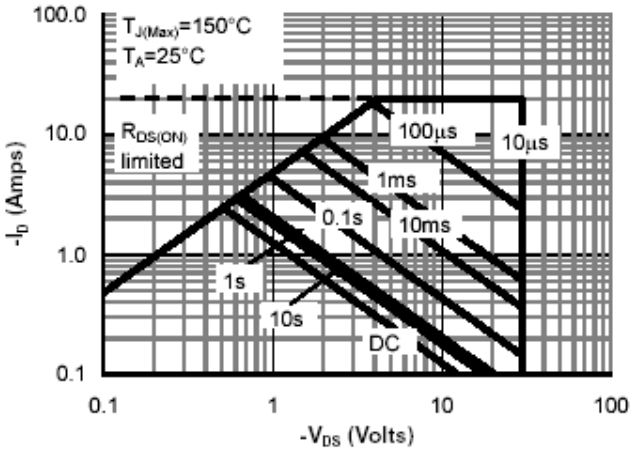


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

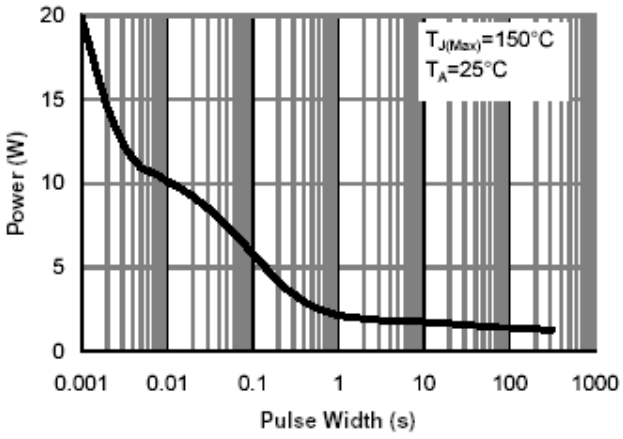


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

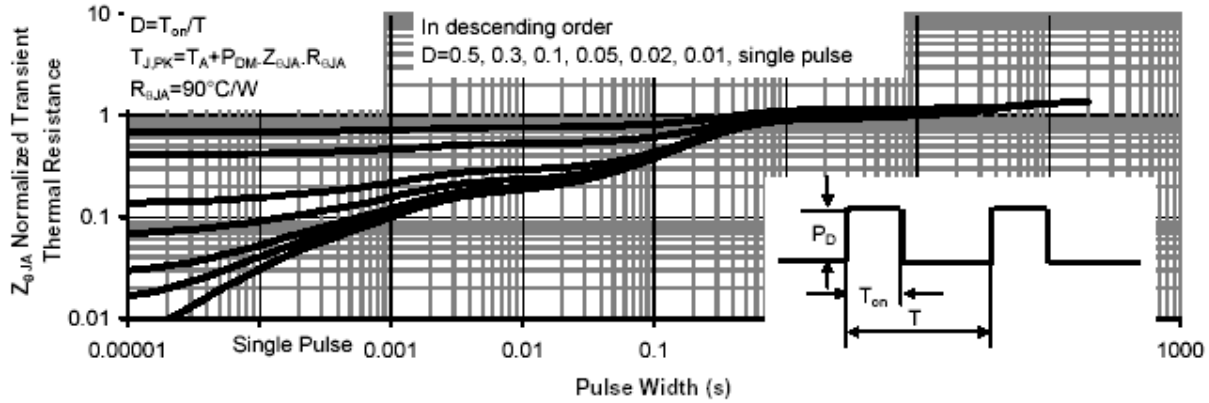


Figure 11: Normalized Maximum Transient Thermal Impedance