

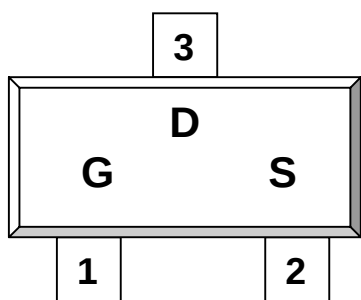
DESCRIPTION

The 3402 is the N-Channel logic enhancement mode power field effect transistor are produced using high cell density, DMOS trench technology.

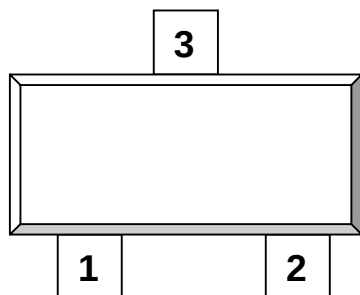
This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other batter powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION SOT-23-3L



1.Gate 2.Source 3.Drain



FEATURE

- 30V/4.0A, $R_{DS(ON)} < 58\text{m-ohm}$
@VGS = 10V
- 30V/2.3A, $R_{DS(ON)} < 65\text{m-ohm}$
@VGS = 4.5V
- 30V/1.5A, $R_{DS(ON)} < 105\text{m-ohm}$
@VGS = 2.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23-3L package design



N Channel Enhancement Mode MOSFET 3402

4.0A

ABSOLUTE MAXIMUM RATINGS (Ta = 25 Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		VDSS	30	V
Gate-Source Voltage		VGSS	+/-12	V
Continuous Drain Current (TJ=150)	TA=25 TA=70	ID	4.0 2.8	A
Pulsed Drain Current		IDM	10	A
Continuous Source Current (Diode Conduction)		IS	1.25	A
Power Dissipation	TA=25 TA=70	PD	1.25 0.8	W
Operation Junction Temperature		TJ	150	
Storage Temperature Range		TSTG	-55/150	
Thermal Resistance-Junction to Ambient		R θ JA	100	/W

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ELECTRICAL CHARACTERISTICS ($T_a = 25$ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.8		1.6	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=12V$			100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=24V, V_{GS}=0V$			1	uA
		$V_{DS}=24V, V_{GS}=0V$ $T_J=55$			10	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \ 4.5V, V_{GS}=10V$ $V_{DS} \ 4.5V, V_{GS}=4.5V$	6 4			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=4.0A$ $V_{GS}=4.5V, I_D=2.3A$ $V_{GS}=2.5V, I_D=1.5A$		0.048 0.053 0.080	0.058 0.065 0.105	Ω
Forward Transconductance	g_{fs}	$V_{DS}=4.5V, I_D=2.8A$		4.6		S
Diode Forward Voltage	V_{SD}	$I_S=-1.25A, V_{GS}=0V$		0.82	1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=15V, V_{GS}=4.5V$ $I_D \equiv 2.0A$		4.2	6	nC
Gate-Source Charge	Q_{gs}			0.6		
Gate-Drain Charge	Q_{gd}			1.5		
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V$ $F=1MHz$		350		pF
Output Capacitance	C_{oss}			55		
Reverse Transfer Capacitance	C_{rss}			41		
Turn-On Time	$t_{d(on)}$	$V_{DD}=15V, R_L=10\Omega$ $V_{GEN}=4.5V, R_G=6\Omega$		2.5		nS
	t_r			2.5		
Turn-Off Time	$t_{d(off)}$			20		
	t_f			4		