N Channel Enhancement Mode MOSFET **3400**

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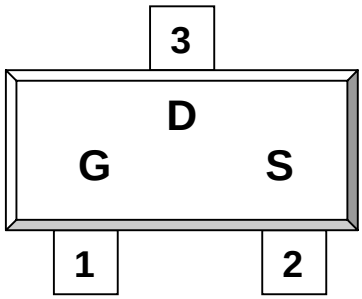
DESCRIPTION

The 3400 is the N-Channel logic enhancement mode power field effect transistor is produced using high cell density, DMOS trench technology.

This high-density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other batter powered circuits where high side switching.

PIN CONFIGURATION

SOT-23-3L



1.Gate 2.Source 3.Drain

FEATURE

- 30V/5.8A, $R_{DS(ON)}$ <38m-ohm @VGS = 10V
- 30V/5.0A, $R_{DS(ON)}$ < 42m-ohm @VGS = 4.5V
- 30V/4.0A, $R_{DS(ON)}$ < 55m-ohm
- @VGS = 2.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23-3L package design

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ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	30	V
Gate-Source Voltage		V_{GSS}	±12	V
Continuous Drain Current (TJ=150℃)	T_A=25℃ T_A=70℃	I_D	5.8 4.9	A
Pulsed Drain Current		I_{DM}	30	A
Power Dissipation	T_A=25℃ T_A=70℃	P_D	1.4 1.0	W
Maximum Body-Diode Continuous Current			2.5	A
Operation Junction Temperature		T_J	-55	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	150	W

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ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	0.7		1.4	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=24V,V_{GS}=0V			1	uA
		V_{DS}=24V,V_{GS}=0V T_J=55℃			5	
On-State Drain Current	$I_{D(on)}$	V_{DS}≦5V,V_{GS}=4.5V	10			A
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=5.8A V_{GS}=4.5V,I_D=5.0A V_{GS}=2.5V,I_D=4.0A		33 37 47	38 42 55	mΩ
Diode Forward Voltage	V_{SD}	I_S=1.0A,V_{GS}=0V		0.7	1.1	V
Dynamic						
Total Gate Charge	Qg	V_{DS}=15V,V_{GS}=4.5V I_D≡5.8A		9.7	12	nC
Gate-Source Charge	Qgs			1.6		
Gate-Drain Charge	Qgd			3.1		
Turn-On Time	$t_{d(on)}$	V_{GS}=10V, V_{DS}=10V, R_L=2.7Ω,V_{GEN}=4.5V		3.3	5	nS
	t_r			4.8	7	
Turn-Off Time	$t_{d(off)}$			26.3	40	
	t_f			4.1	6	

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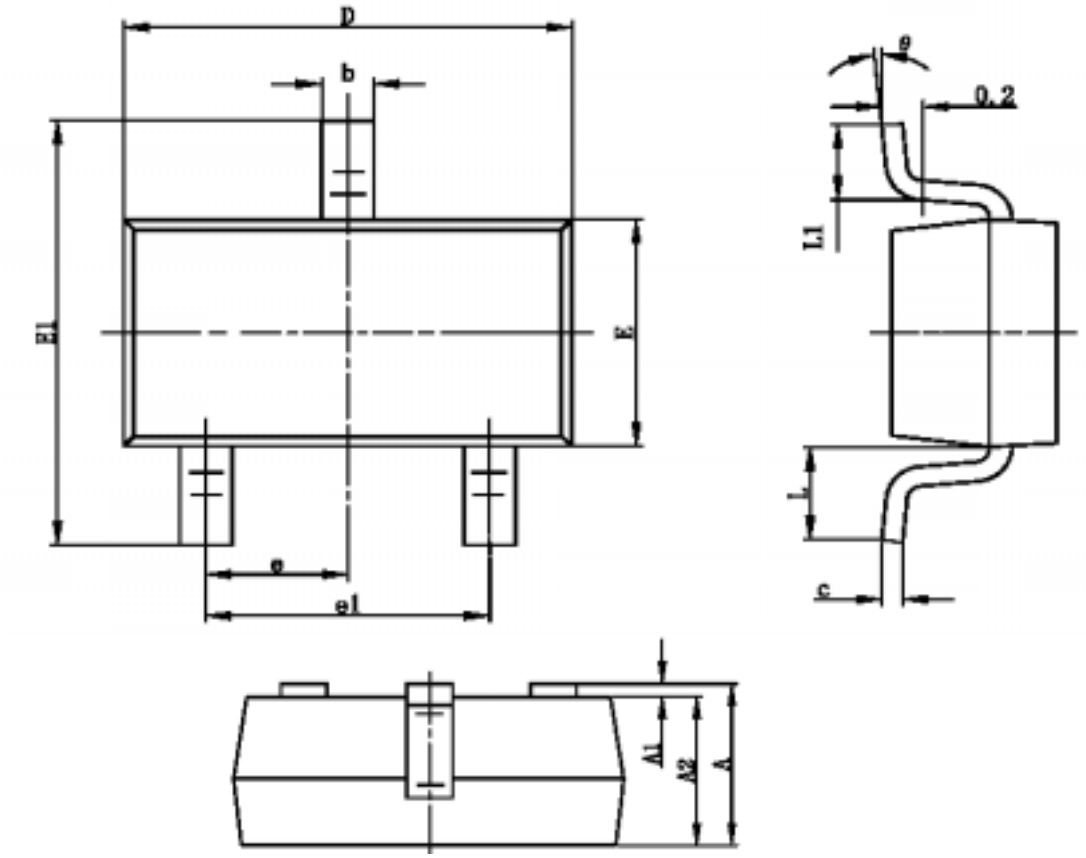
PACKAGE OUTLINE SOT-23-3L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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TYPICAL CHARACTERICTICS

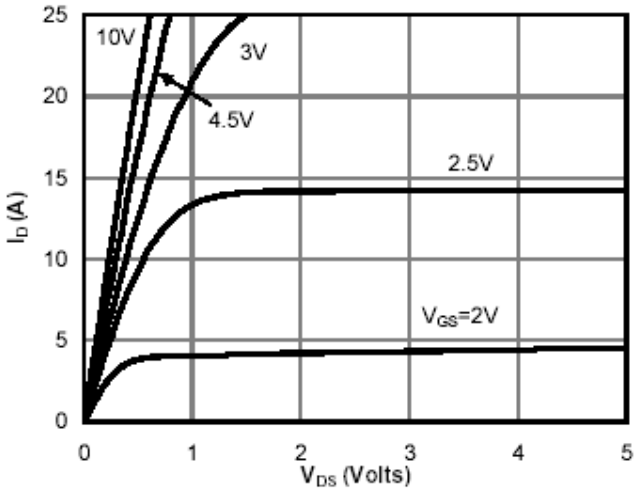

Fig 1: On-Region Characteristics

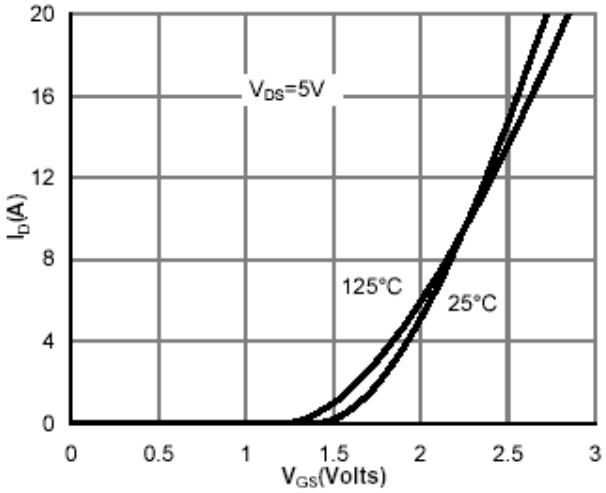

Figure 2: Transfer Characteristics

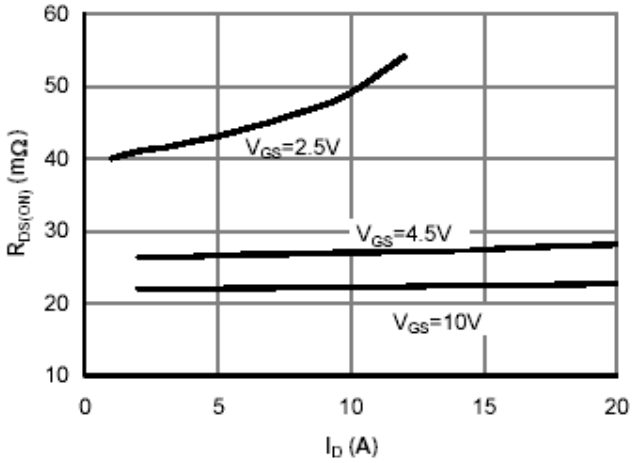

Figure 3: On-Resistance vs. Drain Current and Gate Voltage

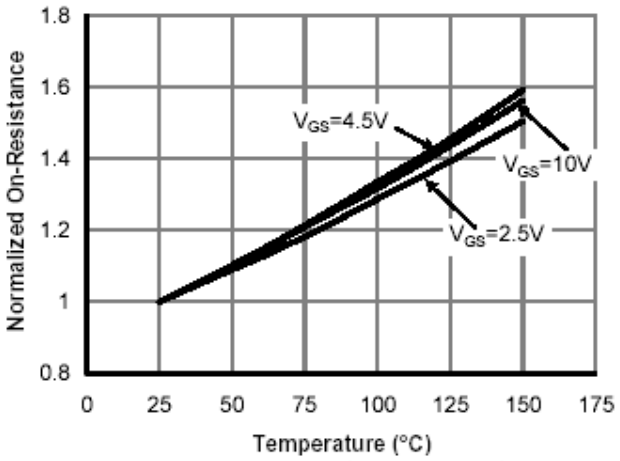

Figure 4: On-Resistance vs. Junction Temperature

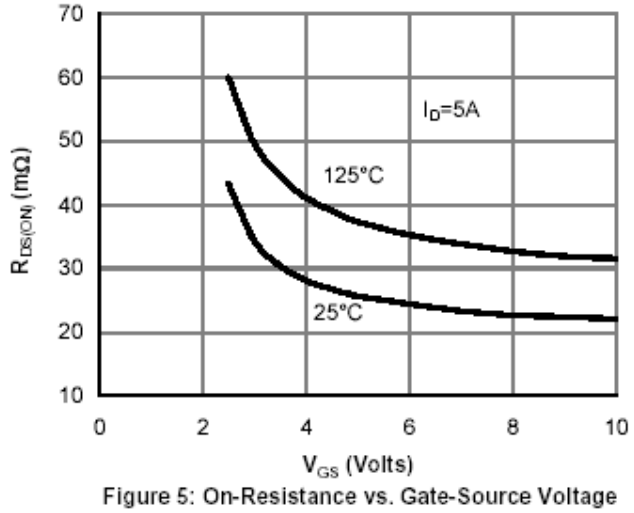

Figure 5: On-Resistance vs. Gate-Source Voltage

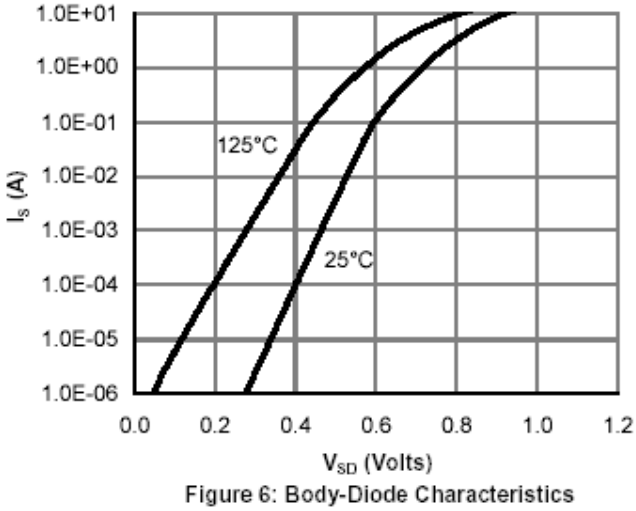

Figure 6: Body-Diode Characteristics

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TYPICAL CHARACTERICTICS

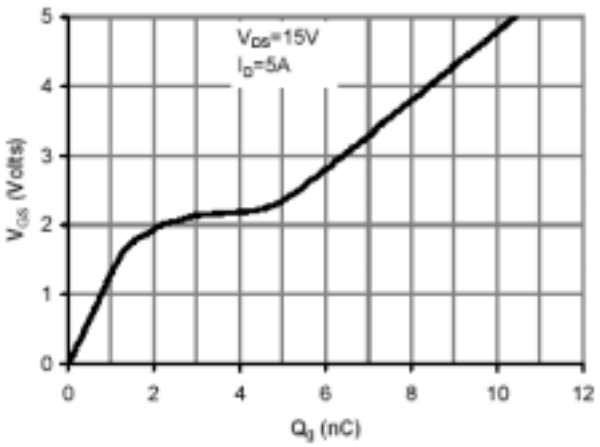

Figure 7: Gate-Charge Characteristics

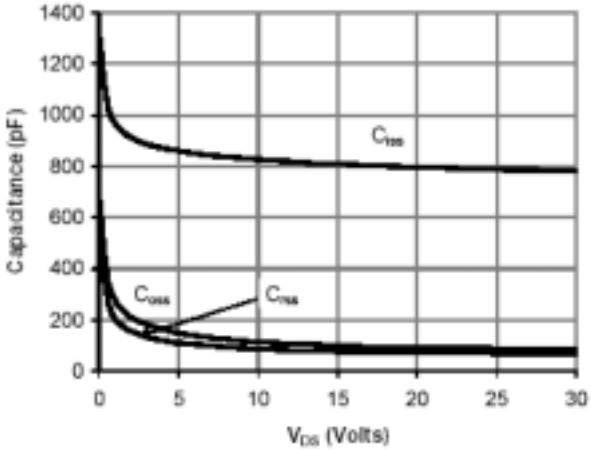

Figure 8: Capacitance Characteristics

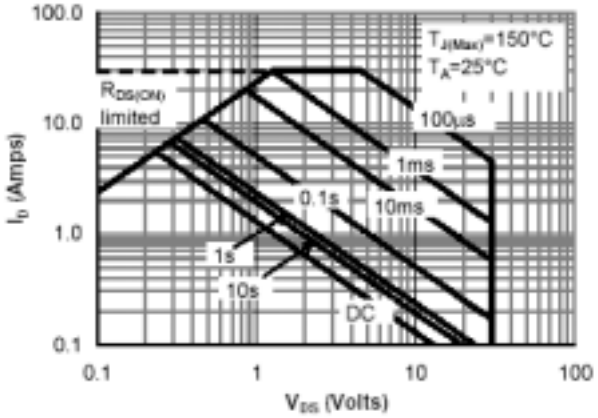

Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

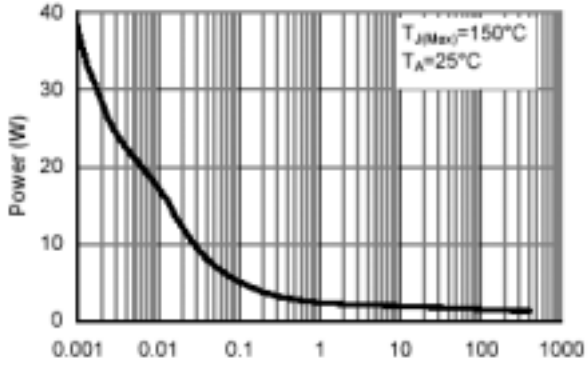

Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

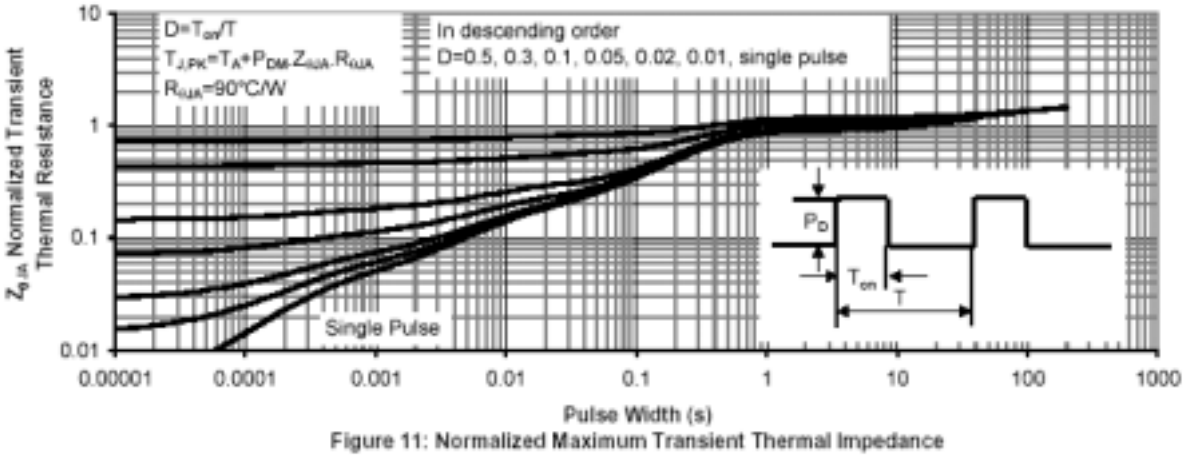

Figure 11: Normalized Maximum Transient Thermal Impedance